Quantum dots and etch-induced depletion of a silicon two-dimensional electron gas

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The controlled depletion of electrons in semiconductors is the basis for numerous devices. Reactive-ion etching provides an effective technique for fabricating both classical and quantum devices. However, Fermi-level pinning must be carefully considered in the development of small devices, such as quantum dots. Because of depletion, the electrical size of the device is reduced in comparison with its physical dimension. To investigate this issue in modulation-doped silicon single-electron transistors, we fabricate several types of devices in silicon-germanium heterostructures using two different etches, CF_4 and SF_6. We estimate the depletion width associated with each etch by two methods: (i) conductance measurements in etched wires of decreasing thickness (to determine the onset of depletion), and (ii) capacitance measurements of quantum dots (to estimate the size of the active region). We find that the SF_6 etch causes a much smaller depletion width, making it more suitable for device fabrication. *© 2006 American Institute of Physics*.
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I. INTRODUCTION

Recently, there has been a renewed interest in modulation-doped, silicon-germanium quantum wells. Modulation-doped field-effect transistors (MODFETs) are potentially attractive for communications applications because of their low noise, low cost, high speed, and compatibility with complementary metal-oxide semiconductor (CMOS) logic.[1] They are also the basis for the high-mobility devices used in quantum dot quantum computing[2–5] and spintronics, where quantum coherence plays a key role. Indeed, it is expected that silicon will exhibit the most desirable coherence properties of any semiconductor (except perhaps carbon) because of its weak spin-orbit coupling and the availability of spin-zero nuclear isotopes.[6,7] In the context of quantum computing, the goal is to fabricate coupled quantum dots containing individual electrons whose spins act as qubits.[4] We have made recent progress towards this goal, overcoming several materials and fabrication challenges.[8] In this paper, we report on Coulomb blockade and single-electron tunneling experiments in which the number of electrons in a silicon quantum dot can be held constant for up to 11 hours. This fulfills an important milestone towards qubit fabrication.

During the 1990's, advances in materials science and growth techniques led to the development of high-quality silicon-germanium quantum wells containing two-dimensional electron gases (2DEGs) with low-temperature electron mobilities of order $6\times10^5\ \mathrm{cm^2/V\,s}$.[9–13] Further progress was hampered by difficulties with leakage currents and parallel conduction paths,[14,15] and unavoidable defects associated with the growth of strained heterostructures. However, spurred on by quantum computing, and technologies such as atomic-layer oxide deposition, some important technological hurdles have been overcome. Reactive ion etching has emerged as an important fabrication tool and a viable alternative to top gating.[16] In this procedure, devices such as quantum dots are formed by physically carving the 2DEG. External side gates for electrostatic control can be fabricated in nearby regions of 2DEG by the same method.

Here, we present evidence for Coulomb blockade in etched quantum dots and we investigate the depletion of the 2DEG near etched surfaces. Etching damages the crystalline structure, potentially introducing dangling bonds and trapped charge. The resulting surface states cause local pinning of the Fermi-level near midgap and, consequently, local modulation of the conduction-band energy. Thus, an electronically depleted region forms near the etch trench. In some cases, edge depletion can present a challenge for fabricating small devices. However, there is also a benefit for quantum devices: because of depletion, the active 2DEG may be physically separated from defects and decoherence-causing centers at the etch boundary.

In this paper, we explore depletion as a tool for fabricating quantum dots. Through a combination of experiments and numerical modeling, we determine the depletion widths in different types of devices. We identify the etch technique that is more conducive for fabricating dots. We also obtain evidence that depletion is nonuniform across structurally nonuniform devices. In Sec. II, we describe sample growth and fabrication techniques, with emphasis on etching. In Sec. III, we describe a set of experiments on relatively simple wire devices, which provide a more direct measurement of

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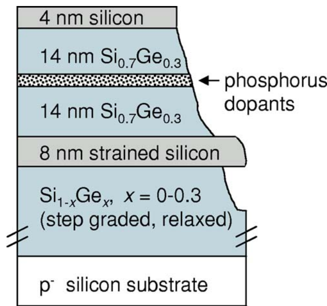

FIG. 1. Cartoon sketch of the heterostructures used in this work. The inhomogeneous region shows the result of reactive ion etching. Etching proceeds more slowly for the silicon active layer, causing a "silicon ledge."

depletion widths. In Sec. IV, we estimate depletion widths in side-gated quantum dots, which exhibit Coulomb blockade and a high degree of stability with respect to charge motion. In Sec. V, we confirm the previous dot estimates through detailed numerical modeling. By comparing the estimated depletion widths, we find that certain etches are more useful for dot fabrication than others. Additionally, the data suggest nonuniform depletion widths in more complicated geometries. In Sec. VI, we investigate this issue in quantum dots by modeling trapped surface charge. In Sec. VII, we draw conclusions and discuss future directions in low-temperature silicon-based quantum devices.

II. GROWTH AND FABRICATION

A Si/SiGe heterostructure was grown by ultrahigh vacuum chemical-vapor deposition (UHVCVD).[10,16] The 2DEG sits near the top of an 8 nm strained silicon quantum well, grown on a strain-relaxed $Si_{0.7}Ge_{0.3}$ buffer layer. The 2DEG is topped with a 14 nm $Si_{0.7}Ge_{0.3}$ spacer layer, and a 14 nm $Si_{0.7}Ge_{0.3}$ supply layer with phosphorus donors. The final structure is capped with 35 Å of silicon, as shown in Fig. 1.

Ohmic contacts were formed with the 2DEG by evaporating Au with 1% Sb and sintering at 400 °C for 10 min. For all experiments described below, the contacts are made prior to reactive-ion etching. Using a hall-bar geometry, the electron density of the 2DEG is found to be 4×10^{11} cm^{-2}, with a mobility of 40 000 cm^2/V s at 2 K.

The devices studied here were fabricated by electron-beam lithography and subsequent CF_4 or SF_6 reactive-ion etching. Extensive studies of this process have shown that for most ion species (including those used here), the etch rate of SiGe increases with germanium content.[17] However, other factors, such as rf power, gas pressure, plasma creation processes, and preferential sputtering of silicon, also affect the etch rate. As a consequence, it is quite difficult to etch uniformly through compositionally varying heterostructures.

For the devices used in this work, the heterostructures were etched to a depth of approximately 120 nm—far deeper than the 2DEG layer. Figure 2 shows scanning electron microscope (SEM) images of our three-gate dot and our six-gate dot. We observe some rounding near the bottom of the trenches, and a prominent silicon ledge of width ~100 nm,

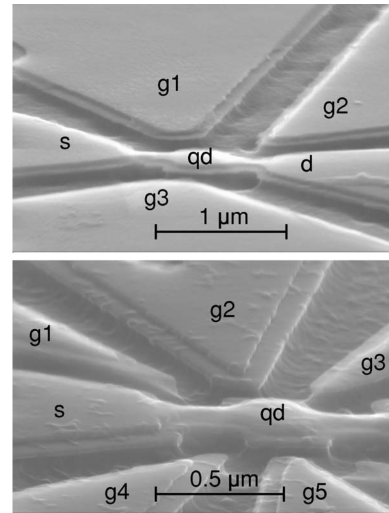

FIG. 2. Scanning electron micrographs of three-gate and six-gate quantum dots studied in this paper. The etched structures include source (s) and drain (d) leads, a quantum dot (qd), and several side gates (g1-g6). (In the lower dot, gate 6 and the drain lie outside the viewing area.)

due to the preferential etching of germanium (see Fig. 1). The undercutting below the silicon ledge is slightly nonuniform.

In the following, we measure the depletion widths from the inner perimeter of the silicon ledge. Inside this ledge, the silicon layer remains mainly intact. However, the contained 2DEG is depleted, due to strain effects and the close proximity to surface trap states. In the unetched, "bulk" regions of our devices, we observe differing depletion widths, depending on the etch.

III. ETCHED WIRES

Nine wires were patterned on two different chips using the CF_4 reactive-ion etch. The wires had different widths, ranging from 200 to 1350 nm, and all the devices were electrically isolated from one another. A typical device is shown in Fig. 3.

As discussed above, the wires have an electrical width smaller than their physical width, due to the depletion of the 2DEG near the etch boundaries. This effect has been studied previously in patterned wires.[18–20] 2DEG depletion can also be modified by passivating the surface states, for example, by growing an oxide layer after etching.[21] We note that oxidation requires high-temperature processing. However, passivation techniques form an interesting direction for future

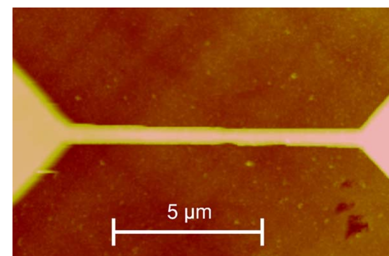

FIG. 3. Atomic force microscope image of a fabricated wire. The darker regions are etched, leaving a narrow channel between the leads.

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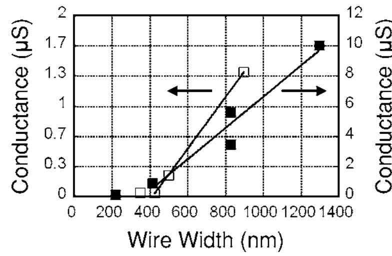

FIG. 4. Conductance vs wire width, for nine wires on two different chips. The different symbols correspond to different chips. The lines show the result of fitting to the nonzero data. The x intercepts give an estimate of $(2\times)$ the depletion width.

work. Here, we investigate unpassivated edge depletion through transport measurements. The conductance of the wires should be proportional to their electrical width. For progressively narrower wires, the 2DEG will eventually cease to conduct. The onset of zero conductance therefore indicates full depletion, and provides an estimate of the depletion width. We assume the depletion width is the same for all the wires on a given chip, due to identical fabrication conditions.

In Fig. 4, the two-point conductance is plotted for each of the wires, as a function of their physical width. Two-point measurements were used instead of four-point measurements in order to maximize the number of wires on a given chip for a given cooldown. Each data point represents an individual wire. The two chips are identified by different symbols. All the measurements are made at 2 K.

As expected, the wire conductance was found to vary approximately linearly with the physical width. A line fit through the higher data points intersects the x axis at about 400 nm for both chips, suggesting a depletion width of about 200 nm on either side of the wires.

IV. QUANTUM DOTS

Several quantum dots were fabricated by reactive ion etching. Here, we report on the two dots shown in Fig. 2. Although similar etching procedures were applied in the two cases, the three-gate dot used the CF_4 etch, while the six-gate dot used the SF_6 etch. All the components of the devices (dot, leads, and gates) were etched from the same 2DEG, with no additional metal top gates. Because of the considerable etch depth (120 nm), we could detect no current flow between the side gates and the dots. However, in other experiments, not reported here, small leakage currents were observed for shallower etch depths (<100 nm). We conjecture that dislocation arms running underneath shallow etch trenches may connect the gates to the dot in such devices. Here, all side gates were contacted ohmically and grounded, unless otherwise noted.

The source and drain leads, together with the quantum dot, are formed from a single structure. However, the necks between the dot and the source-drain leads are designed to give transport resistances slightly larger than the resistance quantum $e^2/h \simeq 25$ kΩ. Thus, the necks form tunnel barriers, even when the side gates are grounded. By adjusting the voltages on different side gates, we can tune the number of electrons on the dot and the tunnel couplings to the source and drain leads. Additional details are provided in Ref. 16.

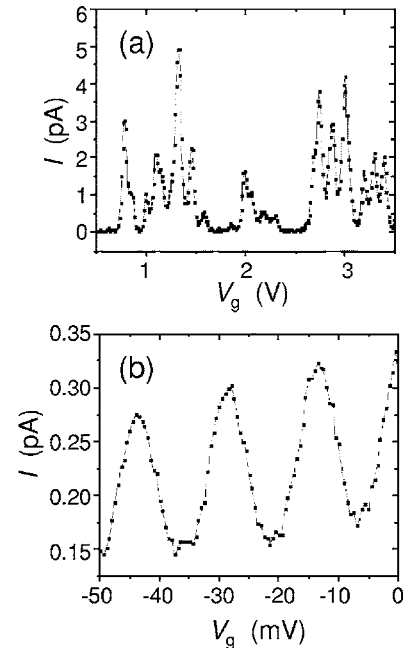

FIG. 5. Coulomb blockade current peaks as a function of gate voltage for (a) the three-gate dot, and (b) the six-gate dot.

Several types of transport measurements are performed on the dots. First, we measure the current through the quantum dot while varying the voltage of a side gate V_g, but holding the bias voltage between the source and drain constant. As shown in Fig. 5, we observe periodic oscillations of the transport current through the quantum dots. The peaks indicate charge quantization in the dots, with successive peaks corresponding to an increment of one electron.[22]

The spacing between consecutive peaks ΔV_g is governed primarily by the plunger gate capacitance, $C_g = e/\Delta V_g$, which determines the energy of the dot relative to the leads. For the three-gate dot, we observe gate capacitances between 0.7 and 1.3 aF.[16] Note that, because of the larger separations (and weaker couplings) between dots and gates in side-gate devices, various combinations of gates can be used for plunging, giving slightly different capacitances. For the six-gate dot, we tie together two of the six gates ($g1$ and $g5$ in Fig. 2) to produce the gate voltage V_g, while grounding the other gates. The resulting data in Fig. 5(b) correspond to a gate capacitance of 11 aF. The larger gate capacitance of the six-gate dot suggests a smaller depletion width. The line shape of the conductance (G) oscillation peaks in the conventional theory of Coulomb blockade[22] is given by $G/G_\infty \simeq 1/[2\cosh^2(\delta/2.5k_BT)]$, where $\delta = e|V_{g,\mathrm{res}} - V_g|C_g/C$ and $V_{g,\mathrm{res}}$ is the resonant gate voltage corresponding to the conductance peak. The relatively wide Coulomb peaks in observed in Fig. 5 reflect the small gate-dot capacitance C_g, compared to the total capacitance C.

A stability plot for the six-gate dot is shown in Fig. 6. The data were taken over an 11 h window, in which no charge switching events were apparent. (A switching event would be marked by a sudden shift of the Coulomb diamonds along the horizontal axis V_g.) This represents a sig-

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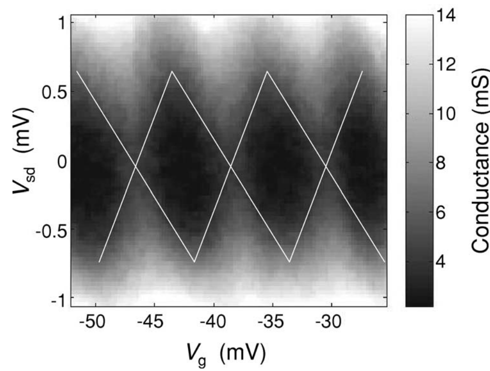

FIG. 6. Stability plot for the six-gate dot, as function of gate and source-drain voltages. Measurements were performed at 300 mK, and show no switching events over the 11 h measurement window. Diamonds are drawn as a guide to the eye.

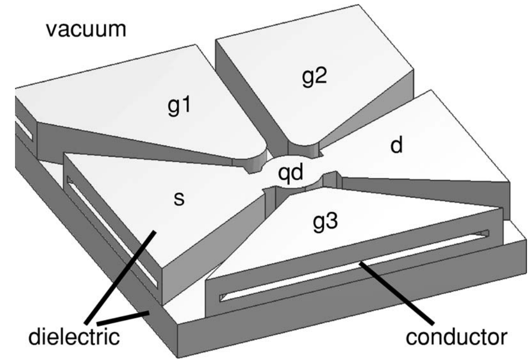

FIG. 7. Simulation geometry for the three-gate dot.

nificant improvement over the six-gate dot, as reported in Ref. 16. In part, we attribute the enhancement to the etching process: the SF_6 etch appears to generate a lower density of surface states, and a corresponding lower frequency of charge switching. However, the measurement was also performed in a 3.6 T magnetic field, known to reduce charge noise. We also tried measuring Coulomb blockade in the CF_4 etched quantum dot in a magnetic field. However, in this case, the Coulomb oscillations were also suppressed.

The shape of the Coulomb diamonds in Fig. 6 provides further information about the dot capacitance C_Σ. In the conventional theory of Coulomb blockade,[23] transport phenomena are explained in terms of the chemical potentials of the N-electron dot, and the left and right leads, $\mu_{\text{dot}}(N), \mu_L$, and μ_R, respectively. At low temperatures, transport across the dot occurs only when $\mu_L > \mu_{\text{dot}}(N) \simeq \mu_{\text{dot}}(N+1) > \mu_R$. Such considerations allow calculations of the shape of the diamonds. The resulting height (from tip to tip) is given by $2e/C_\Sigma$, from which we determine C_Σ. Thus, in Ref. 16, we determined $e^2/C_\Sigma = 3.2$ meV for the three-gate dot. For the six-gate dot, the analysis has large error because of the broad conductance peaks in Fig. 5(b). We find $C_\Sigma = 230$ aF, with a charging energy of 0.70 meV.

We can use these capacitance values to estimate the diameter of the electrically active regions of the quantum dots. Treating the dot as a conducting disk surrounded by an infinite dielectric gives the conductance formula

$$C_\Sigma = 4\epsilon D, \tag{1}$$

where $\epsilon = 11.4\epsilon_0$ is the low-temperature dielectric constant of silicon and D is the diameter of the disk. [Note that in our calculations, we assume materials parameters consistent with silicon, rather than $Si_{0.7}Ge_{0.3}$. This is convenient because (i) the dielectric constants of the two materials differ by only 6% at room temperature,[24] and (ii) low-temperature parameters for SiGe are not well known.] Equation (1) is clearly an approximation. It does not incorporate the complex structure of the real device. In particular, it does not take into account the bending of the electric-field lines at the vacuum interface or the metallic leads. For side-gate devices, the interface has a stronger effect, so that Eq. (1) overestimates C_Σ for a given D. In Sec. V, we treat this problem more carefully using numerical techniques.

From Eq. (1), we can back out an estimate for the electrical width of the dot (as opposed to the actual physical width), using our estimates for the dot capacitance. For the three-gate dot, we find an electrical diameter of 124 nm, compared to a physical width of 720 nm (measured from the silicon ledge). For the six-gate dot, we find an electrical width of 570 nm. Within our error bars, this is the same as its physical width, given by 560 nm. Since the approximations leading to Eq. (1) underestimate the size of the dot, the depletion width in the six-gate dot must be vanishingly small. Thus, the capacitance measurements indicate a much larger depletion width for the three-gate dot.

Based on our measurement of the electron sheet density, far from the etched boundaries, and our estimates of the dot diameters, we can determine the number of electrons in our dots. Using Eq. (1), we find 50 electrons for the three-gate dot. (A better estimate for the dot diameter, in the following section, gives 170 electrons.) For the six-gate dot, we estimate 1000 electrons. We point out that in spite of this large number, single-electron charging effects are still prominent, and the operation is very stable.

V. MODELING OF THE QUANTUM DOT

We can improve on the estimate of Eq. (1) by performing more accurate numerical modeling of the physical device. We specifically consider the three-gate dot of Fig. 2.

The three-dimensional model geometry used in our simulations is shown in Fig. 7. The solid regions correspond to dielectric material, which we model with silicon materials parameters, as discussed above. The exclusions in the solid are metallic, corresponding to undepleted 2DEG regions in the gates and leads. These are properly modeled by fixed-voltage boundary conditions.

Since the depletion width is not known initially, we perform our simulations for many different 2DEG boundaries. A top view of several of the boundaries is shown in Fig. 8. The curves overlay an atomic force microscope (AFM) image of the device. The depletion boundaries are taken to be equidistant from the physical boundaries. This separation corresponds to the depletion width. The necks between the dot and the source-drain leads are assumed to be fully depleted, as consistent with experimental evidence.

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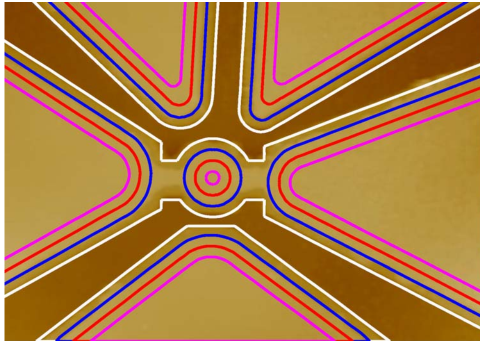

FIG. 8. Top view of the simulation geometry (Fig. 7), showing the etch boundaries (white lines), and the boundaries of the buried 2DEG (black lines). Three depeletion boundaries are shown, corresponding to three different depletion widths. The curves overlay an AFM image of the three-gate dot. The imaged area is 4×4 μm^2.

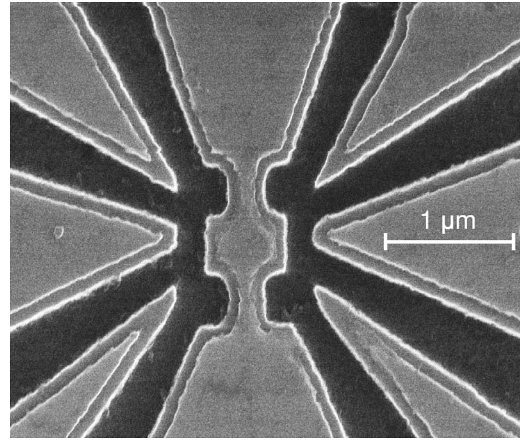

FIG. 9. Atomic force microscope image of the six-gate dot in Fig. 2. The silicon ledge is observed as a ~100 nm rim around each gate.

The capacitance matrix, relating charges to voltages for a system of conductors, is given by[25] $Q_i=\Sigma_{j=1}^n C_{ij}V_j$. The conventional capacitances correspond to the diagonal coefficients C_{ii}. These are computed in our simulation by setting the voltages on all the gates to zero, except for the conductor of interest. Thus, the calculation of C_Σ proceeds by setting the voltage of the quantum dot to 1 V, and the other gates to 0 V. The resulting charge on the quantum dot is equal to its capacitance in units of Farads (F).

In this way, a finite-element analysis[26] obtains the capacitance of the dot as a function of its size. For the experimental value $C_\Sigma=50$ aF, our simulations give a corresponding dot diameter of 233 nm, and a depletion width of 244 nm. This dot size is nearly two times larger than the estimate of Eq. (1). Thus, the numerical result more closely matches the estimate obtained in Sec. III, and confirms our expectation that Eq. (1) should underestimate the true electrical diameter.

VI. DISCUSSION

We have seen that devices fabricated with the CF_4 and SF_6 etches exhibit some important differences. For the CF_4 etch, we observe a significant depletion width, while for the SF_6 etch, the electrical width of the dot is nearly the same as its physical width. We believe these differences can be attributed to a change in the number or the nature of surface charge states caused by the different etching procedures. Yet, there is a contradiction, which is most striking for the SF_6 dot. Although the dot itself remains essentially undepleted, the same cannot be true for the adjacent tunnel barriers. How can we understand this apparently nonuniform depletion?

There are several competing effects which contribute to the observed behavior. The dominant effect is electrostatic. Surface states trap charge originating in the supply layer, forming a band that pins the Fermi level near midgap.[27] Charge trapping causes electric fields, which bend the conduction band locally, causing depletion of the 2DEG. Local electrostatic conditions, such as the position of etched surfaces, affect the local fields, and thus the depletion boundary. Near the tunnel barriers, the total density of the trapped charge is high, due to the geometry of the walls and other nearby gates structures. The depletion width should therefore be nonuniform, and it should be larger in regions such as constrictions, where the sidewalls are closely spaced. By this argument, we should expect to see a larger depletion width in a quantum dot than a wire of equal width. Indeed, this seems to be the case for our experiments.

To model the electrostatics of the surface states, we perform a simulation of the six-gate dot, introducing a uniform charge density on both the top and etched surfaces. (The boundary of the etched structures is taken to be the inner perimeter of the silicon ledge, rather than the outer perimeter; see Fig. 9.) For simplicity, we do not include screening by the 2DEG. Such a model is incomplete, but it provides insight into the effects of surface charge. The computed electrostatic potential gives a good approximation of the locally varying conduction band. In a real device, depletion occurs when the band energy lies above the Fermi level. In our model, depletion occurs when the potential is larger than a particular equipotential line.

Numerically derived depletion boundaries are shown in Fig. 10. The solid line describes a situation most consistent with the SF_6 etch and the six-gate quantum dot. Here, the dot

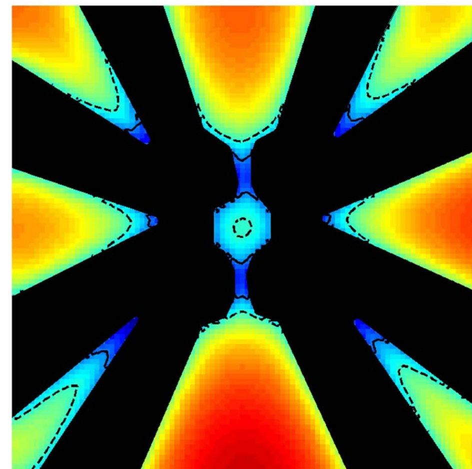

FIG. 10. Color scale results for the electrostatic potential of the six-gate dot (arbitrary units), with etch boundaries at the inner silicon ledge. (See Fig. 9.) The potential is evaluated at the 2DEG layer. Two equipotential lines are shown. The solid curve shows a depletion boundary consistent with capacitance measurements in the six-gate dot.

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and the leads show almost no depletion, while the tunnel barriers are fully depleted. The tips of the side gates are also partially depleted, as most evident in the narrower gates. The dashed line shows a different equipotential corresponding to a larger depletion width. Because Poisson's equation is linear, the same outcome could be obtained with the former equipotential criterion, but a larger surface charge density. The dashed line shows significant depletion of the quantum dot, as well as in the source, the drain, and the side gates. The overall picture is consistent with our measurements in the three-gate dot. We conclude that nonuniform depletions widths arising from electrostatic effects are consistent with conditions observed in the quantum dots studied here. Full depletion is typical in constricted regions such as our tunnel barriers because there are more charged surfaces nearby. Nonconstricted regions, such as the dot or the leads, do not show such enhanced depletion. In this picture, the CF_4 etch data are consistent with a higher density of trapping states, and a correspondingly larger depletion width. However, both etches can cause the tunnel barriers to depelete fully.

In addition to electrostatic effects, quantum kinetic energy can also contribute to the depletion of a narrow tunnel barrier. Typically, such effects become noticeable in devices smaller than ~100 nm. In Fig. 9, we see the minimum barrier width (not including the silicon ledge) can be as small as 80 nm. Treating the barrier as a square well gives the transverse confinement energy $\hbar^2\pi^2/2m^*L_b^2=0.3$ meV, where L_b is the barrier width. If the effective width of the barrier is further reduced by the electrostatic potential from the surface charges, the confinement energy can easily reach several meV. Since this is a characteristic energy scale for quantum dot devices, it is reasonable to assume that confinement effects may also play a role in the depletion of narrow channels.

To facilitate the development of etched devices, it would be desirable to perform simulations that include both electrostatic and quantum-mechanical effects,[28] while allowing charge to move between the trap states, the supply layer, and the 2DEG, to satisfy electrochemical equilibrium. A goal would be to determine the charge profile and the depletion boundary self-consistently. A recent theory by Fogler has made steps in this direction by determining the depletion boundary self-consistently.[29] Charge redistribution and quantum effects are not yet included in the theory.

VII. CONCLUSIONS

We have obtained experimental estimates for the 2DEG depletion width in etched silicon heterostructures by (i) a conductance technique involving etched wires and (ii) a capacitance technique involving etched quantum dots. For the CF_4 etch, the two estimates give 200 and 244 nm, respectively. For the SF_6 etch, we observe a small or vanishing depletion width by the capacitance technique. Thus, SF_6 appears especially useful for fabricating small devices.

By means of simulations, we have shown that the depletion width exhibits local variations in nonuniform etched devices, as consistent with the experimental observations. The shape of the depletion boundary depends on many factors, presenting a challenge for device design. However, we believe that theoretical and numerical design tools should be available in the near future.

The proximity between gates and dots forms an important control issue, since it determines the capacitive coupling of the side gates. For the devices studied here, the minimum separation between undepleted regions in neighboring dots or side gates is about 200 nm in SF_6-etched devices, reflecting the width of the silicon ledge. Although neither of our two etches provide vertical etched walls, we could utilize shallow etches to minimize undercutting, and thus improve our lithographic resolution. It is known that even trenches shallower than the depth of the 2DEG can cause depletion. We believe this level of control will allow an approach to the few electron limit in SiGe quantum dots, which is most conducive for spin physics. In the context of quantum computing, this work forms a promising step towards silicon qubits. Ultimately, such devices will require a fabrication resolution as small as 50–150 nm.[4] We anticipate that improvements in theoretical design tools, passivation, etching, and top-gating techniques will enable continued progress towards this goal.

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[1] S. J. Koester *et al.*, Electron. Lett. **39**, 1684 (2003).
[2] D. Loss and D. P. DiVincenzo, Phys. Rev. A **57**, 120 (1998).
[3] R. Vrijen, E. Yablonovitch, K. Wang, H. W. Jiang, A. Balandin, V. Roychowdhury, T. Mor, and D. DiVincenzo, Phys. Rev. A **62**, 012306 (2000).
[4] M. Friesen, P. Rugheimer, D. E. Savage, M. G. Lagally, D. W. van der Weide, R. Joynt, and M. A. Eriksson, Phys. Rev. B **67**, 121301(R) (2003).
[5] M. Friesen, C. Tahan, R. Joynt, and M. A. Eriksson, Phys. Rev. Lett. **92**, 037901 (2004).
[6] B. E. Kane, Nature (London) **393**, 133 (1998).
[7] E. Yablonovitch, H. W. Jiang, H. Kosaka, H. D. Robinson, D. S. Rao, and T. Szkopek, Proc. IEEE **91**, 761 (2003).
[8] M. A. Eriksson *et al.*, Quantum Inf. Process. **3**, 133 (2004).
[9] F. Schäffler, D. Többen, H.-J. Herzog, G. Abstreiter, and B. Holländer, Semicond. Sci. Technol. **7**, 260 (1992).
[10] K. Ismail, M. Arafa, K. L. Saenger, J. O. Chu, and B. S. Meyerson, Appl. Phys. Lett. **66**, 1077 (1995).
[11] N. Sugii, K. Nakagawa, Y. Kimura, S. Yamaguchi, and M. Miyao, Semicond. Sci. Technol. **13**, A140 (1998).
[12] T. Okamoto, M. Ooya, K. Hosoya, and S. Kawaji, Phys. Rev. B **69**, 041202(R) (2004).
[13] K. Lai, W. Pan, D. C. Tsui, S. Lyon, M. Muhlberger, and F. Schäffler, Phys. Rev. Lett. **93**, 156805 (2004).
[14] S. Kanjanachuchai, T. J. Thornton, J. M. Fernndez, and H. Ahmed, Semicond. Sci. Technol. **13**, 1215 (1998).
[15] A. Notargiacomo, L. Di Gaspare, G. Scappucci, G. Mariottini, F. Evangelisti, E. Giovine, and R. Leoni, Appl. Phys. Lett. **83**, 302 (2003).
[16] L. J. Klein *et al.*, Appl. Phys. Lett. **84**, 4047 (2004).
[17] Y. Zhang, G. S. Oehrlein, E. de Frsart, and J. W. Corbett, J. Vac. Sci. Technol. A **11**, 2492 (1993).
[18] M. Holzmann, D. Többen, G. Abstreiter, M. Wendel, H. Lorenz, J. P. Kotthaus, and F. Schäffler, Appl. Phys. Lett. **66**, 833 (1995).
[19] R. G. van Veen, A. H. Verbruggen, E. van. der. Drift, F. Schäffler, and S. Radelaar, Semicond. Sci. Technol. **14**, 508 (1999).
[20] E. Giovine *et al.*, Nanotechnology **12**, 132 (2001).
[21] Y. Takahashi, A. Fujiwara, M. Nagase, H. Namatsu, K. Kurihara, K.

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Iwadate, and K. Murase, Int. J. Electron. **86**, 605 (1999).
[22] L. P. Kouwenhoven, C. M. Marcus, P. L. McEuen, S. Tarucha, R. M. Westervelt, and N. S. Wingreen, in *Mesoscopic Electron Transport*, edited by L. L. Sohn, L. P. Kouwenhoven, and G. Schön (Kluwer, Dordrecht, 1997), p. 105.
[23] M. H. Devoret and H. Grabert, in *Single Charge Tunneling*, 2nd ed., edited by H. Grabert and M. H. Devoret (Wiley, New York, 1992), p. 1.
[24] R. Ahuja, C. Persson, A. F. da Silva, J. S. de Almeida, C. M. Araujo, and B. Johansson, J. Appl. Phys. **93**, 3832 (2003).
[25] J. D. Jackson, in *Classical Electrodynamics*, 2nd ed. (Wiley, New York, 1975).
[26] We use the commercial finite element software FEMLAB (www.comsol.com).
[27] S. M. Sze, in *Physics of Semiconducting Devices*, 2nd ed. (Wiley, New York, 1981).
[28] C. W. J. Beenakker and H. van Houten, Solid State Phys. **44**, 1 (1991), and reference therein.
[29] M. M. Fogler, Phys. Rev. B **69**, 245321 (2004).

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